

REMARKS

Claims 1-30 are pending in the present application, and stand rejected. By this amendment, claims 1, 11, 20-30 are amended. This application continues to include claims 1-30.

Claim 20 was amended to insert a period at the end of the sentence. Original claims 22-30 reference the system of claim 21, although claim 21 is directed to a data packet communication device. Accordingly, claims 22-30 have been amended to replace "system" with --device-- to avoid any potential antecedent issues associated therewith.

The Examiner objected to the disclosure stating that the title of the invention is not descriptive. Applicants respectfully disagree since the current title is DATA PACKET COMMUNICATION DEVICE, and the claims are directed to a method, system, and apparatus associated with a data packet communication device. Reconsideration is respectfully requested. In the event the Examiner continues to believe that the title is not descriptive, Applicants would appreciate a suggestion for an acceptable title.

Claims 1-3, 5-15, 19-25 and 28-30 were rejected under 35 USC §102(b) as being anticipated by Harriman, et al. (U.S. Patent No. 5,898,687). Applicants respectfully request reconsideration of the rejection of claims 1-3, 5-15, 19-25 and 28-30 in view of the following.

Harriman, et al. discloses a multicast engine of a shared-memory switching fabric circuit that increases the replication rate of data elements destined for multicast connections within a network switch by manipulating address information relating to those elements. FIG. 1 is a schematic block diagram of a network switch 100 comprising a shared-memory switching fabric circuit 110 for transferring information among input ports 102, output ports 104 and a central processing unit (CPU) 106. The switch 100 is preferably an asynchronous

transfer mode (ATM) switch configured with N input ports and N output ports. (Column 3, lines 46-52). At the heart of the switching fabric 110 is a shared memory store unit 112 having storage locations typically composed of random access memory (RAM) devices addressable by the CPU and ports. (Column 3, line 66-column 4, line 2). Coupled to the shared memory are a conventional extraction circuit 114 that apporions each cell received at the switching fabric 110 into its constituent payload and header information fields, and a conventional assemble circuit 116 that appends these fields to form a reconstituted ATM cell prior to transferring the cell to the output ports. (column 4, lines 7-12). Upon receiving a cell from the source port 102, the switching fabric 110 extracts the payload data from the cell, stores it in its shared memory 112 over line 115 and records the memory address of that payload location in an address pointer 128. (Column 4, lines 35-39). The input stage 210 of the multicast engine 200 preferably comprises a buffer memory that stores information prior to manipulation by the output stage 230. (Column 4, lines 65-67).

Claim 1, as amended, is directed to a method of processing data packets, and recites, in part, receiving a plurality of the data packets at a selected node and extracting only pertinent information from the data packets while ignoring non-pertinent information from the data packets, the pertinent information being pertinent to said selected node. Support for the amendment of claim 1 may be found, for example, in Applicants' specification at page 4, lines 5-18. While Harriman, et al. discloses processing a plurality of data packets, Harriman, et al. does not disclose, teach or suggest "extracting only pertinent information from the data packets while ignoring non-pertinent information from the data packets" as recited in claim 1, as amended. Accordingly, claim 1 is believed allowable in its present form.

Claims 2, 3 and 5-10 depend, directly or indirectly, from claim 1, and are believed to be in condition for allowance in view of their dependence from otherwise allowable base claim 1.

In addition, claims 2, 3 and 5-10 are believed to be patentable in their own right.

For example, claim 2 recites, in part, “wherein said extracting and generating steps are performed without use of a storage memory.” (Emphasis added). In contrast, as disclosed in Harriman, et al. with respect to Fig. 1, upon receiving a cell from the source port 102, the switching fabric 110 extracts the payload data from the cell, stores it in its shared memory 112 over line 115 and records the memory address of that payload location in an address pointer 128. (Column 4, lines 35-39). Also, the input stage 210 of the multicast engine 200 preferably comprises a buffer memory that stores information prior to manipulation by the output stage 230. (Column 4, lines 65-67). Accordingly, claim 2 is believed to be patentable in its own right.

Claim 11, as amended, is directed to a data packet communication system, and recites a peripheral device; and a filter device connected to said peripheral device, said filter device being configured to receive a plurality of data packets and identify only pertinent information in said data packets while ignoring non-pertinent information from said data packets, said pertinent information being pertinent to said peripheral device. Claim 11 is believed allowable for substantially the same reasons set forth above with respect to claim 1.

Claims 12-15, 19 and 20 depend, directly or indirectly, from claim 21, and are believed to be in condition for allowance in view of their dependence from otherwise allowable base claim 11.

In addition, claims 12-15, 19 and 20 are believed to be patentable in their own right.

For example, claim 13 recites, in part, wherein said filter device is memoryless. In contrast, as disclosed in Harriman, et al. with respect to Fig. 1, upon receiving a cell from the source port 102, the switching fabric 110 extracts the payload data from the cell, stores it in its shared memory 112 over line 115 and records the memory address of that payload location in an address pointer 128. (Column 4, lines 35-39). Also, the input stage 210 of the multicast engine 200 preferably comprises a buffer memory that stores information prior to manipulation by the output stage 230. (Column 4, lines 65-67). Accordingly, claim 13 is believed to be patentable in its own right.

Claim 21, as amended, is directed to a data packet communication device, and recites, in part, a filter device configured to receive a plurality of data packets and identify only pertinent information in said data packets while ignoring non-pertinent information from said data packets. Claim 21 is believed allowable for substantially the same reasons set forth above with respect to claim 1.

Claims 22-25 and 28-30 depend, directly or indirectly, from claim 21, and are believed to be in condition for allowance in view of their dependence from otherwise allowable base claim 21.

In addition, claim 22-25 and 28-30 are believed to be patentable in their own right.

For example, claim 23 recites, in part, wherein each of said filter device and said packet generator is memoryless. In contrast, as disclosed in Harriman, et al. with respect to Fig. 1, upon receiving a cell from the source port 102, the switching fabric 110 extracts the payload data from the cell, stores it in its shared memory 112 over line 115 and records the memory address of that payload location in an address pointer 128. (Column 4, lines 35-39). Also, the input stage 210 of the multicast engine 200 preferably comprises a buffer memory

that stores information prior to manipulation by the output stage 230. (Column 4, lines 65-67). Accordingly, claim 23 is believed to be patentable in its own right.

In view of the above, Applicants respectfully request that the rejection of claims 1-3, 5-15, 19-25 and 28-30 be withdrawn.

Claims 4, 16-18, 26 and 27 were rejected under 35 USC §103(a) as being unpatentable over Harriman, et al. (U.S. Patent No. 5,898,687) in view of Krishnan, et al. (U.S. Pub. No. 2003/0007489 A1). Applicants respectfully request reconsideration of the rejection of claims 4, 16-18, 26 and 27 in view of the following.

Applicant has submitted along with this Amendment a Declaration Under 37 C.F.R. §1.131(a), in which Applicants declare that the Applicants invented the claimed subject matter corresponding to claims 4, 16-18, 26 and 27 prior to July 9, 2001, thus antedating Krishnan, et al., and removing Krishnan, et al. as a reference under 35 U.S.C. §103(a) relative to claims 4, 16-18, 26 and 27. Further, Harriman, et al. does not disclose, teach or suggest the subject matters of claims 4, 16-18, 26 and 27. Thus, claims 4, 16-18, 26 and 27 are believed patentable in their own right.

In addition, claims 4, 16-18, 26 and 27 are believed patentable in view of their dependence from an otherwise allowable base and/or intervening claim.

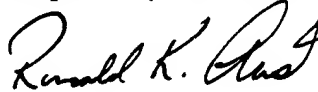
Accordingly, Applicants respectfully request that the rejection of claims 4, 16-18, 26 and 27 be withdrawn.

For the foregoing reasons, Applicants submit that the present application is in condition for allowance in its present form, and Applicants respectfully request withdrawal of all rejections and allowance of the claims.

In the event Applicants have overlooked the need for an extension of time, an additional extension of time, payment of fee, or additional payment of fee, Applicants hereby conditionally petition therefor and authorize that any charges be made to Deposit Account No. 20-0095, TAYLOR & AUST, P.C.

Should any question concerning any of the foregoing arise, the Examiner is invited to telephone the undersigned at (317) 894-0801.

Respectfully submitted,



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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: MS Amendments, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on: October 12, 2005.

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October 12, 2005

Date